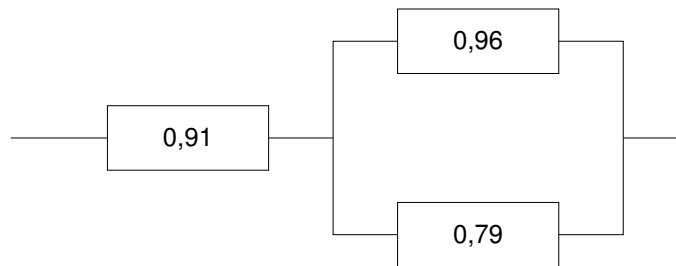


1. Construct a  $128 \times 8$  concentrator using  $8 \times 8$  crossbars and  $4 \times 1$  multiplexers. The concentrator should be non-blocking in the sense that any 8 out of the 128 inputs can be connected to the 8 outputs.
2. What is the reliability of the system below? What is the optimal place to add a spare module (reliability = 0.93) and what is the new reliability that is achieved?



3. Consider a system with two redundant units in parallel. Both the active and standby units are energised. For both units the failure rate is  $\lambda = 1/100$  days and the repair rate is  $\mu = 1/6$  hours. If the active unit fails, the standby unit takes its tasks and the failed unit undergoes repairs. Make a Markov model for the system, form the equilibrium equations (as functions of  $\lambda$  and  $\mu$ ) and solve the state probabilities for each of the states. Note that if the both units have failed they are repaired consecutively.
4. Consider the use of 2.4 Gbit/s fiber optics link for transporting voice circuits (each requiring 64 kbit/s capacity) via ATM.
  - (a) What is the minimum size of the VCI?
  - (b) What is the minimum size of the VCI if the 2.4 Gbit/s link is divided into 16 STM-1 ATM channels?
  - (c) Why can we achieve a reduction in the size of the VCI by having smaller channels? What is the hidden cost?
5. Consider a 16 slot ATM switch where each slot can be equipped with a multiport line interface card (LIC). Possible LIC configurations are 1xSTM-16, 4xSTM-4 and 16xSTM-1. Each LIC contains only a single RIT at input port controller, i.e., in multiport LIC IPC and RIT are shared. A single line in RIT contains only new VPI and VCI values and output port index. Each line should be read in a single cycle.
  - (a) What is the required memory speed and bus width for RIT?
  - (b) How many connections can be supported by a single port if RIT is implemented using a single 16 Mbit SRAM device? How many SRAMs are required to cover the whole VPI/VCI space?