1. A time switch is implemented using the principle given below:

   - Incoming time-slots are written cyclically into a switch memory (SM)
   - Output logic reads cyclically control memory (CM), which contains a pointer for each output time-slot

   Inputs and outputs as well as read/write logic of the memories are expected to be in synchronism.

   What are the required speeds of SM and CM if the switching is dimensioned to support 120 input and output E1-links. What are required memory sizes of SM and CM? What about the sizes of input and output buffers? Suppose that SM and CM are shared by all E1s and that there is a memory slot for each time-slot.

2. Consider a 3-stage circuit switched symmetric Clos switching matrix with 512 input lines. Each input has an average holding time of 260 s and input rate of 1/320 1/s.

   (a) The input is divided into 32 blocks of type 16xk, where k is number of 2nd stage blocks. Use Lee's approximation to find out such k that the blocking probability is < 0.001. What is the total number of switching points?

   (b) What the value of k and the number of the switching points if the switch must be strictly non-blocking?

3. Consider the recursive construction of an $N \times N$ rearrangeably non-blocking Clos network using only $p \times p$ crossbars only.

   (a) Compute the number of crosspoints as a function N and p.

   (b) For large N, show that $p = 3$ minimises the crosspoint count.

4. Compute the crosspoint complexity, logical depth (the number of logical gates in a path), and fan-out (the number of logical gates driven by the input or by any gate in the network) for the following networks.

   (a) The full $N \times N$ crosspoint switch.

   (b) The three stage rearrangeable Clos network constructed using $\sqrt{N} \times \sqrt{N}$ switches.

   (c) The Benes network.