

1. Consider a 16 slot ATM switch where each slot can be equipped with a multiport line interface card (LIC). Possible LIC configurations are 1xSTM-16, 4xSTM-4 and 16xSTM-1. Each LIC contains only a single RIT at input port controller, i.e., in multiport LIC IPC and RIT are shared. A single line in RIT contains only new VPI and VCI values and output port index. Each line should be read in a single cycle.
 - (a) What is the required memory speed and bus width for RIT?
 - (b) How many connections can be supported by a single port if RIT is implemented using a single 16 Mbit SRAM device? How many SRAMs are required to cover the whole VPI/VCI space?
2. Consider the same system as in previous task.
 - (a) The switch fabric uses 64-byte frame in which the cells are encapsulated. What is the required throughput for the switch fabric?
 - (b) Latest DDR-SRAM technology can support cycle rates up to 400 MHz. How fast LICs can be constructed using these devices and what is the fastest SDH frame structure that can be supported (provided that RIT speed is the limiting factor)?
3. Hardware based IP address lookup can be realised using two level multibit stride. Consider a system where 1st level stride is 24-bit and 2nd level is 8-bit (slide 10-65).
 - (a) Suppose that we are using DRAM devices having 85 ns random access time to implement the address lookup system. The system is pipelined and thus one lookup operation is completed at each memory cycle on the average. What is the throughput of a router using this system in worst case conditions? (Hint: under which conditions the arrival rate of IP datagrams is highest for an arbitrary bitrate?)
 - (b) The performance requirements are relaxed so that the average IP datagram length of 200 octets can be used to derive the performance requirements. How many 1 Gbit/s Ethernet interfaces can supported? (NB: GbE ports operate in full-duplex mode, so neither carrier extension nor burst mode is used).
4. Consider the same system as in previous task.
 - (a) How many memory accesses are required to 1st level memory to update 8, 16, and 24 bit IP address prefixes?
 - (b) Let's suppose that an average prefix update mix contains 10% 8-bit, 30% 16-bit, and 60% 24-bit prefix updates. At what prefix update rates the number of memory accesses caused by updates exceeds that of normal address lookups?
 - (c) At which update rate the system saturates, i.e., consumes all resources for prefix updates?