PDH Switches

Switching Technology S38.165
**http://www.netlab.hut.fi/opetus/s38165**

PDH switches

- General structure of a telecom exchange
- Timing and synchronization
- Dimensioning example

PDH exchange

- Digital telephone exchanges are called SPC (Stored Program Control) exchanges
  - controlled by software, which is stored in a computer or a group of computers (microprocessors)
  - programs contain the actual intelligence to perform control functions
  - software divided into well-defined modular blocks, which makes the system less complicated to maintain and expand
- Main building blocks
  - subscriber interfaces and trunk interfaces
  - switch fabric
  - switch/call control

Basic blocks of a PDH exchange
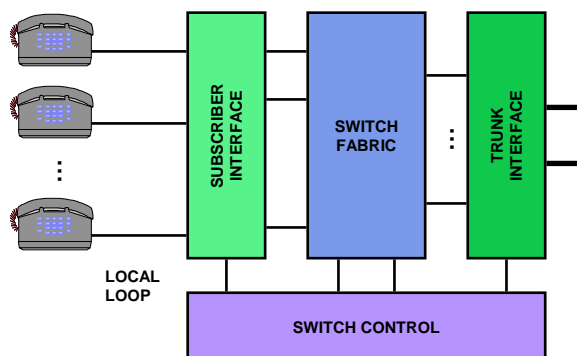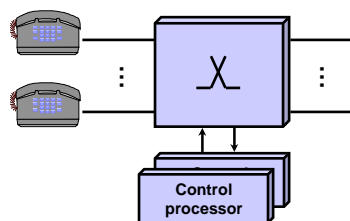
Switch control

- **Centralized**
  - all control actions needed to set up/tear down a connection are executed in a central processing unit
  - processing work normally shared by a number of processors
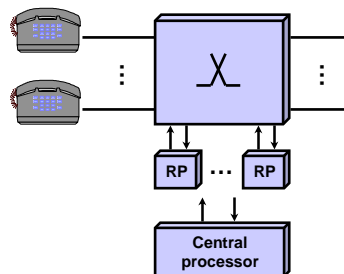 - hierarchical or non-hierarchical processor architecture
- **Distributed**
  - control functions are shared by a number of processing units that are more or less independent of one another
  - switching device divided into a number of switching parts and each of them has a control processor

Switch control (cont.)

Centralized non-hierarchical processor system

Control units usually doubled or tripled

Centralized hierarchical processor system

RP - Regional Processor

Switch control (cont.)

**Distributed control
with independent switching parts**

Switching part with control processor	Switching part with control processor
Switching part with control processor	Switching part with control processor
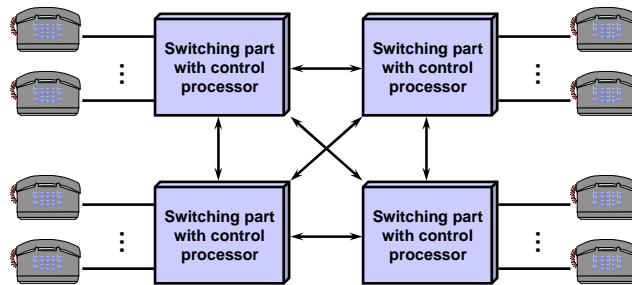
Example construction of a PDH exchange

SUBSCRIBER INTERFACES   SWITCHING & CALL CONTROL   TRUNK INTERFACES

NT

NT

SWITCH FABRIC

ET

ET

AUX

CONTROL PROCESSOR
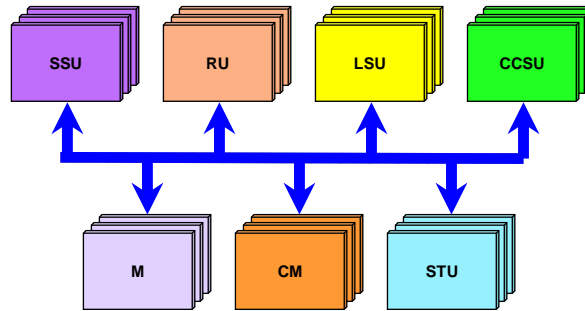
ADMINISTRATION COMPUTER
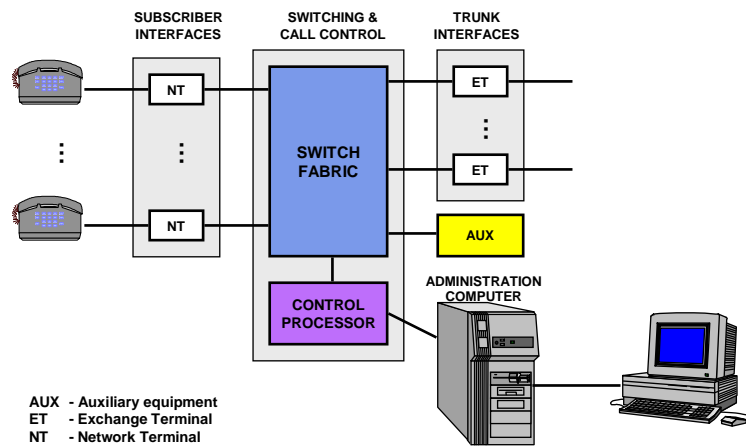
AUX   - Auxiliary equipment
ET   - Exchange Terminal
NT   - Network Terminal

Example of call control processing

CCSU	- Common Channel Signaling Unit	**RU** - Registering Unit
CM	- Central Memory	**SSU** - Subscriber Stage Unit
LSU	- Line Signaling Unit	**STU** - Statistics Unit
M	- Marker	

DX200 / Nokia

Call processing units

- **Common Channel Signaling Unit (CCSU)**
  - processes SS7 signaling messages
- **Central Memory (CM)**
  - common central memory of the different control units
- **Line Signaling unit (LSU)**
  - processes line signaling information
- **Marker (M)**
  - connection (channel) control
- **Register Unit (RU)**
  - registers for information such as call/customer related billing
- **Subscriber Stage Unit (SSU)**
  - subscriber stage control (incl. subscriber signaling)
- **Statistics Unit (STU)**
 - statistical information such as call durations and outage periods

Hierarchical control software

Software systems in the control part:
- signaling and call control
- charging and statistics
- maintenance software

Control of connections:
- calls should not be directed to faulty destinations
- faulty connections should be cleared
- detected faulty connections must be reported to far-end if possible

Administration programs

Call control programs

Signaling message processing
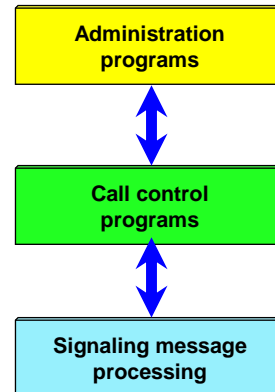
Switching part

- Main task of a switching part is to connect an incoming time-slot to an outgoing one – unit responsible for this function is called a group switch
- Control system assigns incoming and outgoing time-slot, which are reserved by signaling, on associated physical links
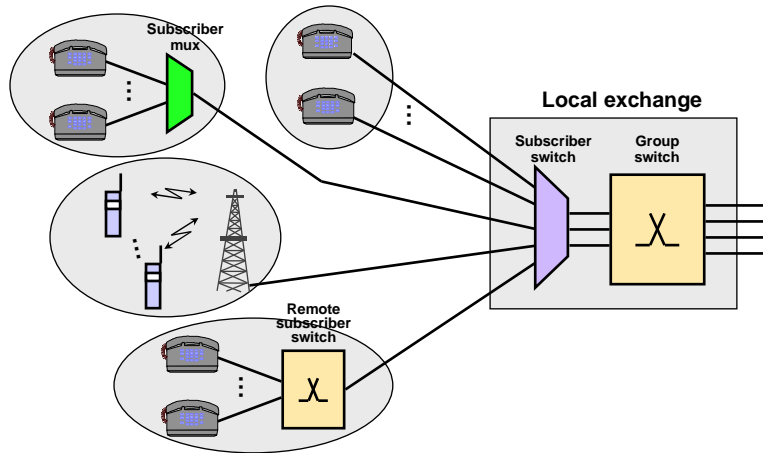 => need for time and space switching
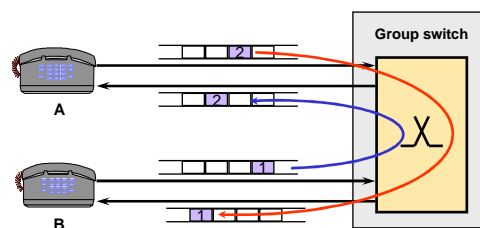
Group switch implementations

- Group switch can be based on a space or time switch fabric
- Memory based time switch fabrics are the most common ones
  - flexible construction
  - due to advances in IC technology suitable also for large switch fabrics
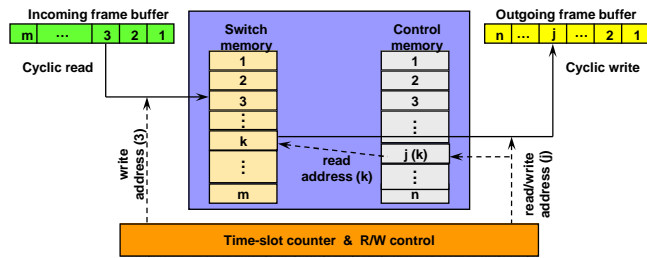
Subscriber connections

Typical subscriber connections and trunk lines

- **Subscriber connections**
  - conventional twisted pair serving, e.g., an analog 3 kHz voice channel or 2B+D digital ISDN connection
  - radio link serving, e.g., an analog voice channel (NMT) or a digital GSM voice/data channel
  - E1, …, E3 links connecting business users with a number of voice channels
- **Trunk lines**
  - standard PDH links (E1, …, E4)
  - standard SDH links (STM-1, ..., STM-16) carrying standard PDH/PCM signals

Subscriber and trunk interface

- **Subscriber interface**
  - on-hook/off-hook detection, reception of dialed digits
  - check of subscriber line, power supply for subscriber line
  - physical signal reception/transmission, A/D-conversion
  - concentration
- **Trunk interface**
  - timing and synchronization (bit and octet level) to line/clock signal coming from an exchange of higher level of hierarchy
  - frame alignment/frame generation
  - multiplexing/demultiplexing

Example of telephone network hierarchy

International transit level

National transit level

Regional transit level

Tandem level

Local exchange
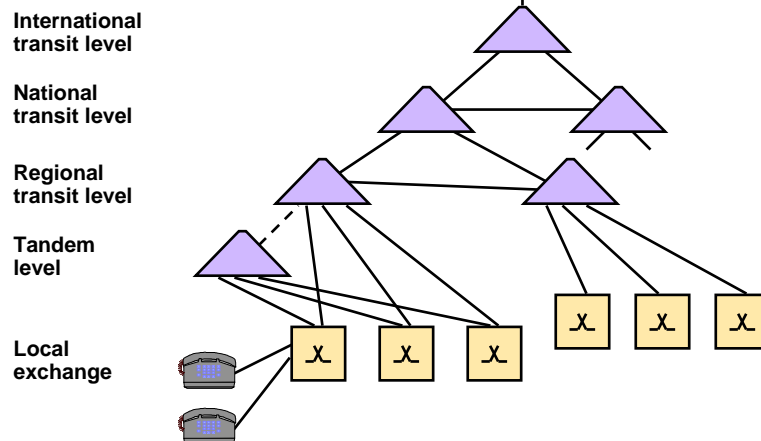
Network synchronization

Need for synchronization

- Today's digital telecom networks are combination of PDH and SDH technologies, i.e. TDM and TDMA utilized
- These techniques require that time and timing in the network can be controlled, e.g., when traffic is added or dropped from a bit stream in an optical fiber or to/from a radio-transmitted signal
- The purpose of network synchronization is to enable the network nodes to operate with the same frequency stability and/or absolute time
- Network synchronism is normally obtained by applying the **master-slave timing principle**

Network synchronization

Methods for network synchronization

- Distribute the clock over special synchronization links
    - offers best integrity, independent of technological development and architecture of the network
- Distribute the clock by utilizing traffic links
    - most frequently used (master-slave network superimposed on the traffic network)
- Use an independent clock in each node
    - expensive method, but standard solution in international exchanges
- Use an international navigation system in each node
    - GPS (Global Positioning System) deployed increasingly
    - independent of technological development and architecture of network
- Combine some of the above methods

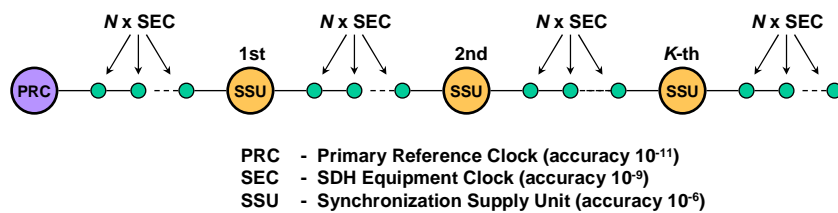## Master-slave synchronization over transport network

International level

High-stability reference clocks

Transit level

Local exchange level

Remote subscriber switch
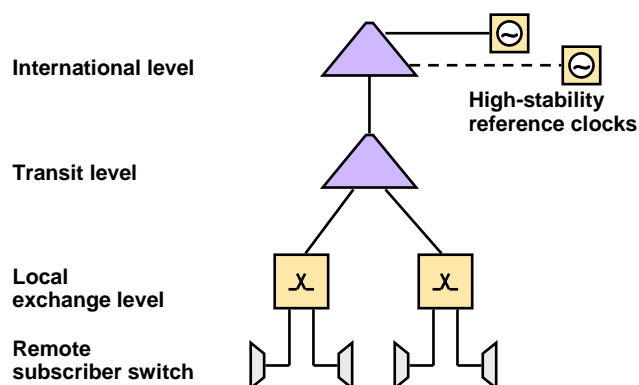
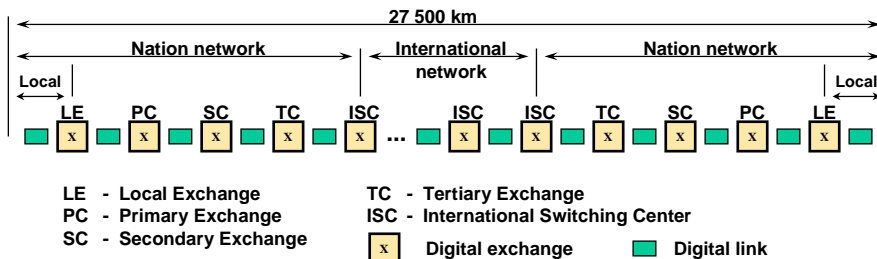**ITU-T Recommendations G.810, G.811, G.812, G.812, G.823**

SDH synchronization network reference chain

- As the number of clocks in tandem increases, synchronization signal is increasingly degraded
- To maintain clock quality, it is important to specify limit to the number of cascaded clocks and set limit on degradation of the synchronization signal
- Reference chain consists of *K* SSUs each linked with *N* SECs
- Provisionally *K* and *N* have been set to be *K*=10 and *N*=20
  - total number of SECs has been limited to 60

N x SEC N x SEC N x SEC N x SEC

1st   2nd   *K*-th

PRC   SSU   SSU   SSU

PRC - **Primary Reference Clock (accuracy 10^{-11})**
SEC - **SDH Equipment Clock (accuracy 10^{-9})**
SSU - **Synchronization Supply Unit (accuracy 10^{-6})**

## PDH synchronization reference connection

- End-to-end timing requirements are set for the reference connection
- Link timing errors are additive on the end-to-end connection
- By synchronizing the national network at both ends, timing errors can be reduced compared to totally plesiochronous (separate clock in each switch) operation
- International connections mostly plesiochronous

27 500 km

Nation network   **International network**   **Nation network**

Local   Local

LE   PC   SC   TC   ISC ... **ISC   ISC   TC   SC   PC   LE**

LE - **Local Exchange**   **TC** - **Tertiary Exchange**
PC - **Primary Exchange**   **ISC** - **International Switching Center**
SC - **Secondary Exchange**   **x**   **Digital exchange**   ▢ **Digital link**

Types of timing variation

- **Frequency offset**
  - steady-state timing difference - causes buffer overflows
- **Periodic timing differences**
  - jitter (periodic variation > 10 Hz)
  - wander (periodic variation < 10 Hz)
- **Random frequency variation** cased by
  - electronic noise in phase-locked loops of timing devices and recovery systems
  - transients caused by switching from one clock source to another
- Timing variation causes
  - slips (= loss of a frame or duplication of a frame) in PDH systems
  - pointer adjustments in SDH systems => payload jitter
  - => data errors

## Visualization of jitter and wander
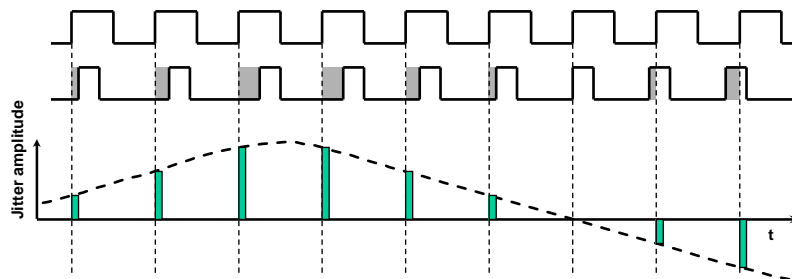
Timing variation measures

- **Time interval error (TIE)**
  - difference between the phase of a timing signal and phase of a reference (master clock) timing signal (given in ns)
- **Maximum time interval error (MTIE)**
  - maximum value of TIE during a measurement period
- **Maximum relative time interval error (MRTIE)**
  - underlying frequency offset subtracted from MTIE
- **Time deviation (TDEV)**
  - average standard deviation calculated from TIE for varying window sizes

Maximum time interval error

- Maximum of peak-to-peak difference in timing signal delay during a measurement period as compared to an ideal timing signal
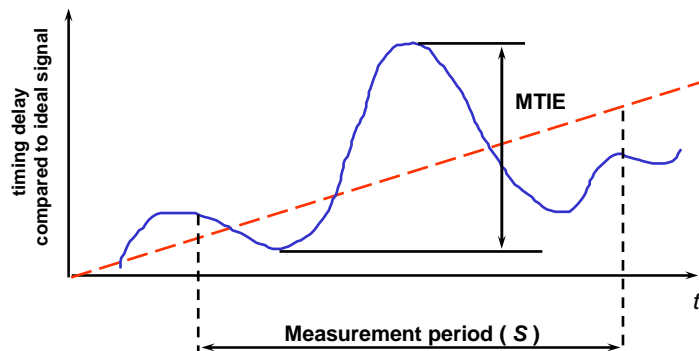
MTIE limits for PRC, SSU and SEC

Clock source	Time-slot interval [ns]	Observation interval
PRC	25 ns $0.3t$ ns 300 ns $0.01t$ ns	$0.1 < t < 83$ s $83 < t < 1000$ s $1000 < t < 30\,000$ s $t > 30\,000$ s
SSU	25 ns $10t$ ns 2000 ns $433t^{0.2} + 0.01t$ ns	$0.1 < t < 2.5$ s $2.5 < t < 200$ s $200 < t < 2\,000$ s $t > 2\,000$ s
SEC	250 ns $100t$ ns 2000 ns $433t^{0.2} + 0.01t$ ns	$0.1 < t < 2.5$ s $2.5 < t < 20$ s $20 < t < 2\,000$ s $t > 2\,000$ s

ETS 300 462-3

Occurrence of slips

- Slips occur on connections whose timing differs from the timing signal used by the exchange
- If both ends of a connection are internally synchronized to a PRC signal, theoretically slips occur no more frequently than once in 72 days
- In a **reference connection,** a slip occurs theoretically once in 72/12 = 6 days or if national segments are synchronized once in 72/4 = 18 days
- Slip requirement on an end-to-end connection is looser:

Average frequency of slips	Share of time during one year
≤ 5 slips / 24h	98.90 %
5 slips/ 24 h …. 30 slips/ 1h	< 1 %
≤ 10 slips / 1h	< 0.1 %

Slip calculation example

Show that two networks with single frame buffers and timed from separate PRCs would see a maximum slip rate of one slip every 72 days

Solution:

- Timing accuracy of a PRC clock is 10^{-11}
- Let the frequencies of the two ends be f_1 and f_2
- In the worst case, these frequencies deviate from the reference clock f_o by $10^{-11} \times f_o$ and those deviations are to different directions
- Let the frequencies be $f_1 = (1 + 10^{-11}) f_o$ and $f_2 = (1 - 10^{-11}) f_o$
- Duration of bits in these networks are $T_1 = 1/f_1$ and $T_2 = 1/f_2$

Slip calculation example (cont.)

Solution (cont.):

- During one bit interval, the timing difference is $|T_1 - T_2|$ and after some N bits the difference exceeds a frame length of 125 µs and a slip occurs $=> N|T_1 - T_2| = 125 \times 10^{-6}$
  $=> N = 125 \times 10^{-6} / [|T_1 - T_2|] = 125 \times 10^{-6} / [|(1/f_1 - 1/f_2)|]$
- Inserting $f_1 = (1 + 10^{-11}) f_o$ and $f_2 = (1 - 10^{-11}) f_o$ into the above equation, we get $=> N = 125 \times 10^{-6} f_o (1 - 10^{-22})/(2 \times 10^{-11}) = 62.5 \times 10^5 \times f_o$
- Multiplying N by the duration (T_b) of one bit, we get the time (T_{slip}) between slips
- In case of E1 links, $f_o = 2.048 \times 10^6/s$ and $T_b = 488$ ns. Dividing the obtained T_{slip} by 60 (s), then by 60 (min) and finally by 24 (h) we get the average time interval between successive slips to be 72.3 days

Synchronization of a switch

Synchronization sub-system in an exchange

- Supports both plesiochronous and slave mode
- Clock accuracy is chosen based on the location of the exchange in the synchronization hierarchy
  - accuracy decreases towards the leaves of the synchronization tree
- Synchronizes itself automatically to several PCM signals and chooses the most suitable of them (primary, secondary, etc.)
- Implements a timing control algorithm to eliminate
  - instantaneous timing differences caused by the transmission network (e.g. switchovers - automatic replacement of faulty equipment with redundant ones)
  - jitter
- Follows smoothly incoming synchronization signal

Synchronization of a switch (cont.)

Exchange follows the synchronization signal

- Relative error used to set requirements
  - maximum relative time interval error MRTIE$\leq$1000 ns (S$\geq$ 100s)
- Requirement implies how well the exchange must follow the synchronization signal when the input is practically error free
- When none of the synchronization inputs is good enough, the exchange-clock automatically switches over to plesiochronous operation
- In plesiochronous mode MRTIE$\leq (aS + 0.5bS^2 + c)$ ns
- Timing system monitors all incoming clock signals and when a quality signal is detected, the system switches over back to slave mode (either manually by an operator command or automatically)

Stability of an exchange clock

- Clock stability is measured by aging (= b)
  - temperature stabilized aging in the order of $n \times 10^{-10}$/day
- MRTIE $\leq (aS + 0.5bS^2 + c)$ ns
  - S = measurement period
  - a = accuracy of the initial setting of the clock
 - b = clock stability (measured by aging)
  - c = constant

	Transit node clock	Local node clock
a	0.5 - corresponds to an initial frequency shift of 5×10^{-10}	10.0 - corresponds to an initial frequency shift of 1×10^{-8}
b	1.16×10^{-5} - corresponds to aging of 10^{-9}/days	2.3×10^{-4} - corresponds to aging of 2×10^{-8}
c	1000	1000

MRTIE in an exchange
(plesiochronous mode)
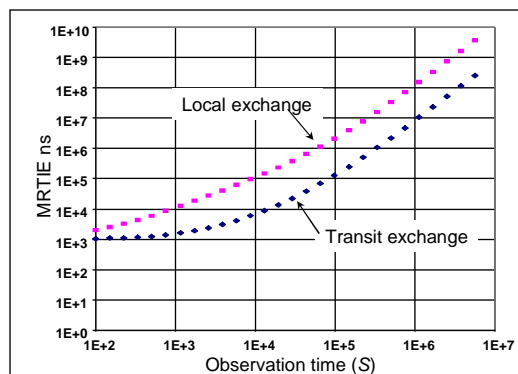
Duration of a time-slot in an E1 PCM-signal is 3.9 µs and duration of a bit is 488 ns.

Example of SRAM based PDH switch fabric
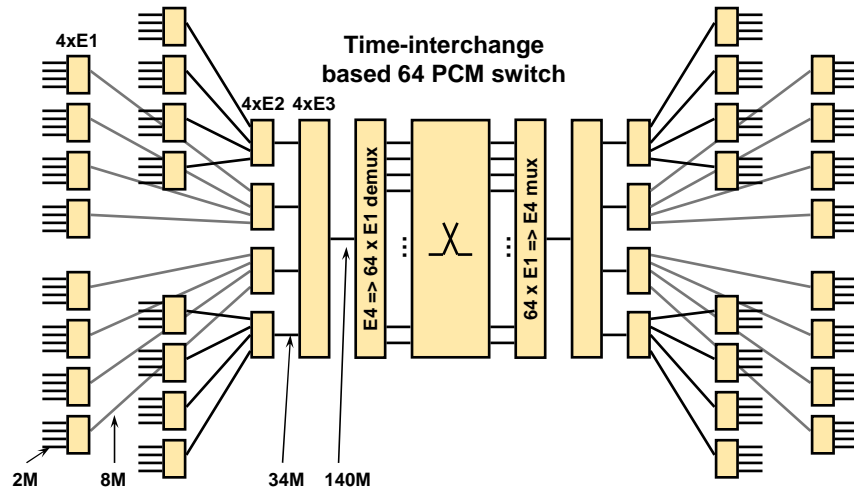
Example of SRAM based PDH switch fabric (cont.)

Memory size and speed requirement:

- Switch memory (SM) and control memory (CM) are both single chip solutions
- Size of both SM and CM $\geq$ 64x32 octets = 2048 octets
- Number of SM write and read cycles during a frame interval (125 μs) is 2x64x32 = 4096
- Access cycle of SM should be $\leq$ 125 μs / 4096 = 30,5 ns
- Number of CM write and read cycles during a frame interval (125 μs) is 1x64x32 = 2048
- Access cycle of CM should be $\leq$ 125 μs / 2048 = 61 ns

PDH bit rates and related bit/octet times

Hierarchy level	Time-slot interval [ns]	Bit interval [ns]
E1/2M	3906	488
E2/8M	947	118
E3/34M	233	29
E4/140M	57.4	7.2

- When time-slots turn into parallel form (8 bits in parallel) memory speed requirement decreased by a factor of 8
- Present day memory technology enables up to 256 PDH E1 signals to be written to and read from a SRAM memory on wire speed

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# Properties of full matrix switches

Pros
- strict-sense non-blocking
- no path search - a connection can always be written into the control memory if requested output is idle
- multi-cast capability
- constant delay
- multi-slot connections possible

Cons
- switch and control memory both increase in square of the number of input/outputs
- broadband - required memory speed may not be available

Make full use of available memory speed

- At the time of design, select components that
  - give adequate performance
  - will stay on the market long enough
  - are not too expensive (often price limits the use of the fastest components)
- To make full use of available memory speed, buses must be fast enough
- When increasing required memory speed, practical bus length decreases (proportional to inverse of speed)
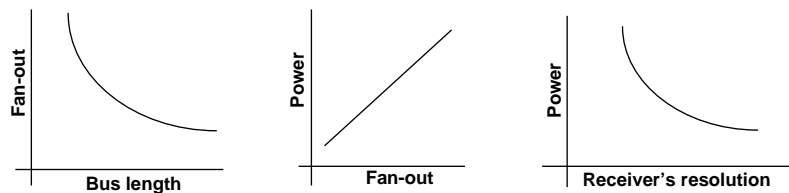
$/SRAM

DRAM: 20 ... 70 ns

5 ns   20 ns

Bus Bit-rate

Memory speed

Bus bit-rate

Length of a bus
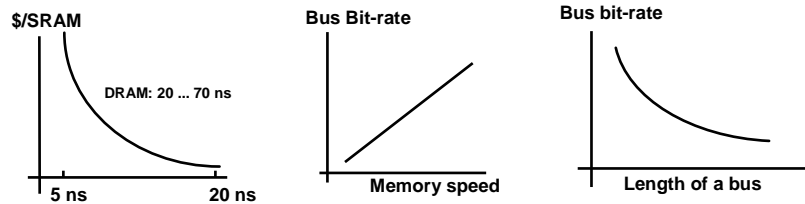
Power consumption - avoid heating problem

- Power consumption of an output gate is a function of
  - inputs connected to it (increased number of inputs => increased power consumption)
  - bit rate/clock frequency (higher bit rate => increased power consumption)
  - bus length (long buses inside switch fabric => increased power consumption and decreased fan-out)
- Increase in power consumption => heating problem
- Power consumption and heating problem can be reduced, e.g. by using lower voltage components (higher resolution receivers)
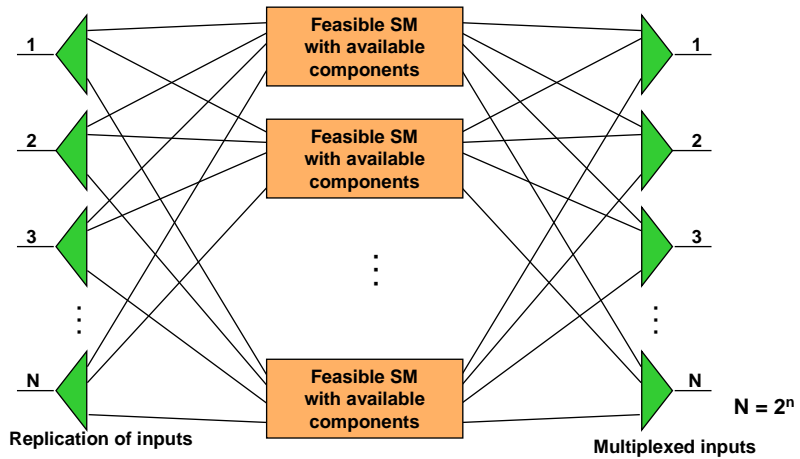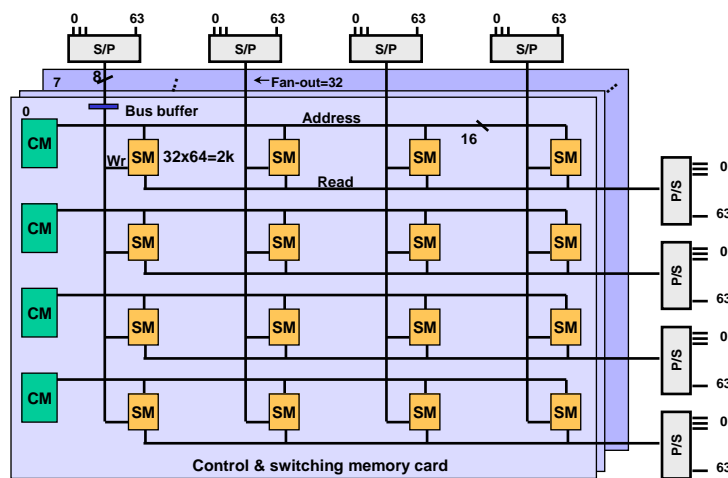
Fan-out

Bus length

Power

Fan-out

Power

Receiver's resolution

Logical structure of a full matrix switch

1
2
3
⋮
N

Feasible SM with available components

Feasible SM with available components

⋮

Feasible SM with available components

1
2
3
⋮
N

$N = 2^n$

Replication of inputs

Multiplexed inputs

Example of a matrix switch (DX200)

0   63   0   63   0   63   0   63

S/P   S/P   S/P   S/P

7   8   ⋮   ←Fan-out=32

0   Bus buffer   Address

CM   Wr SM 32x64=2k   SM   SM   16   SM

Read

CM   SM   SM   SM   SM

CM   SM   SM   SM   SM

CM   SM   SM   SM   SM

P/S   0
      63
P/S   0
      63
P/S   0
      63
P/S   0
      63

Control & switching memory card

Example of a matrix switch (cont.)

- **S/P** (Serial/Parallel conversion) - incoming time-slots are turned into parallel form to reduce the speed on internal buses
- **P/S** (Parallel/Serial conversion) - parallel form output signals converted back to serial form
- 64 PCM S/P-P/S pairs implemented on one card, which is practical because PCMs are bi-directional
- One switch block can serve max 4 S/P-P/S pairs - which is chosen based on required capacity (64, 128, 192 or 256 E1/PCMs)
- One S/P+P/S pair feeds max 8 parallel switch blocks - chosen based on the required capacity in the installation (n * 256 E1/PCM's)
- Max size of the example DX200-system fabric is 2048 E1/PCM's
- Currently, a bigger matrix (8K E1/PCM's) is available, slightly different SRAMs are needed, but principle is similar

Example of a matrix switch (cont.)

- A time-slot is forwarded from an S/P to all parallel switch blocks and (in each switch block) it is written to all SMs along the vertical bus
- A single time-slot replicated into max 4x8=32 locations
- Data in CMs directs storing of a time-slot in correct positions in SMs
- CM also includes data which directs reading of a correct time-slot to be forwarded to each output time-slot on each output E1 link
- CM includes a 16-bit pointer to a time-slot to be read
  - 2 bits of CM content point to an SM chip and
  - 5 + 6 = 11 bits point to a memory location on an SM chip
  - remaining 3 bits point to (source) switch block

Example of a matrix switch (cont.)

- Number of time-slots to be switched during a frame (125 µs):
  - 8x4x64x32 = 65 536 time-slots (= 64 kbytes)
- Each time-slot stored in 4 SMs in each of the 8 switch blocks
  => max size of switch memory 8x4x65 536 = 2097152 (= 2 Mbytes)
- Every 32nd memory location is read from SM in a max size switch
  => average memory speed requirement < 31 ns (less than the worst case requirement 64x32 write and 64x32 read operations during a 125 µs period)
- Control memory is composed of 4x4 control memory banks in each of the 8 switch blocks and each memory bank includes 2.048 kwords (word= 2 bytes) for write and 2.048 kwords for read control, i.e. max CM size is 8x4x4x8kbytes = 1048576 bytes (= 1 Mbytes)

Growth of matrix

256 PCM

512 PCM