Performance Evaluation of ATM Switching Systems

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Abstract

This paper investigates performance evaluation of Asynchronous Transfer Mode (ATM) switching systems: Private Branch Exchanges (PBX), switches and cross-connects. The performance evaluation of ATM switching systems is not as straightforward as one might expect. This is due to the fact that performance can be seen from different angles. The measurements presented in this paper include: throughput, switching delay, switching delay variation, buffer size, accuracy of the Usage Parameter Control (UPC) procedure and cell discarding under overload situation. These properties have been evaluated through a series of measurements. The measurements are quite general although they have been carried out only against Fore System's ASX-200 PBX. The main value of this study is in comparison of different measurement techniques rather than in the actual results. The results depend on the environment but the techniques are valid in general.

1. Introduction

ATM has its roots in packet communications although it has basic properties of circuit switching. To mix the good sides of circuit and packet switching and to avoid weaknesses is not trivial. ATM, as it is today, is a compromise between the efficiency of packet switching and the latency of circuit switching. These two factors contribute to the overall performance of ATM switching systems.

To evaluate the performance of ATM switching systems is not as straightforward as one might expect. This is due to the fact that performance can be seen from different angles. The performance can be considered as the raw ability to transfer cells through the switching matrix, the efficiency of call handling subsystems or even as the efficiency of traffic management. These definitions are all important but none of them is adequate alone. Usually when performance is considered the perspective is in the area of network performance. Network performance covers, as stated in ITU Recommendation I.350, call set-up and release and actual quality of switching as shown in Table 1.

Call Setup		
Connection setup delay	Misrouting ratio	Connection setup denial ratio
Information transfer		
Cell transfer delay	Cell transfer delay variation	Cell transfer capacity
Accuracy of Information transfer		
Cell error ratio	Cell block error ratio	Cell misinsertion rate
Dependability		
	Cell loss ratio	
Call Release		
Connection release delay	Misreleased connection ratio	Release failure ratio

Table 1 Modified performance parameters for switching systems [1]

Quality is evaluated by measuring the delays and errors that occur during switching. These definitions of performance do not cover the management part of a switching system. Partially in overload situations traffic management is very important to the overall performance.

Performance is evaluated at certain points of the reference configuration. These points can be seen in two different ways. One is network performance (NP) and the other is Quality of Service (QoS). QoS takes into account the end device characteristics which usually are much weaker than those of the network equipment. [1]

The measurement unit used in this work is the ADTECH AX/4000 which is a VXI-bus based measurement unit. In the information transfer parameter and the cell discard measurements the source model used at the probe source was periodic cells with the peak cell rate (PCR) 4831 cell/s.

2. Information transfer

2.1 Cell transfer delay

Cell Transfer Delay (CTD) is actually a parameter of an ATM connection to be chosen and not very suitable for usage for evaluation of switching systems. In case of switching system a more suitable term is the switching delay which is the delay of the raw cell transfer from input to output. Switching delays accumulate in the network along connection constituting the real CTD.

Inside the switch the different components have different tasks which by their operation contribute to the total delay. First is input module which has heavy task of preprosessing the incoming cells. It has to cope with cells arriving at full wire speed and separate cells belonging to the management and signalling unit. The input module is responsible for the parameter control. The switching fabric has responsibility of buffering and routing. Under heavy load there can be blocking inside the switch which has strong influence on the total switching delay. The output module has only few tasks. It is responsible for adding operation

and maintenance cells as well as signalling cells to the traffic stream. This rather stochastic process constitutes a small random delay component.

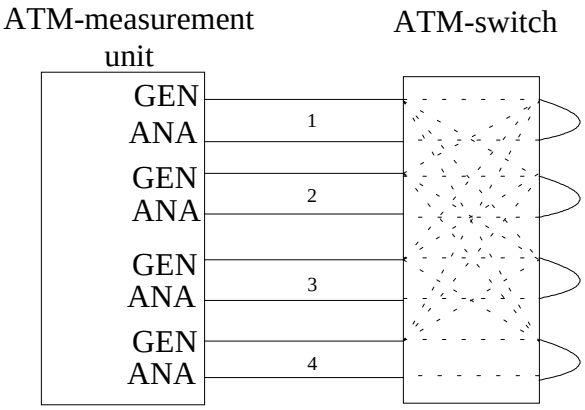


Figure 1 Connection diagram for switching delay measurement

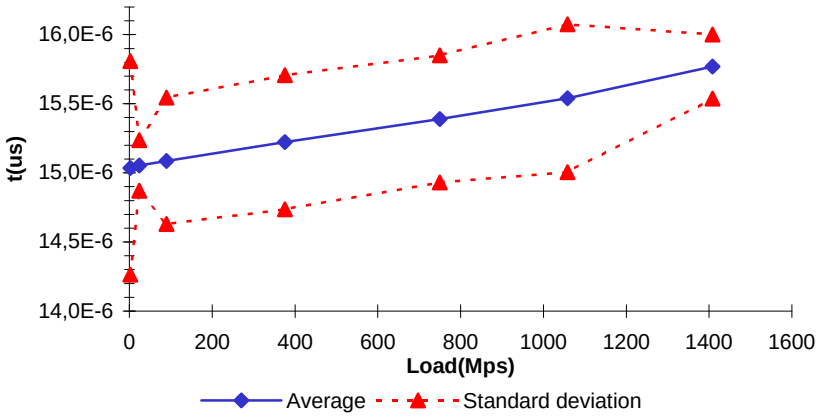


Figure 2 Switching delay as function of background load

2.2 Cell Delay Variation

Cell Delay Variation (CDV) has the same background as cell transfer delay. This time we are more interested in the variability of the switching time than the average nature of it. CDV can be evaluated from the arriving cell stream using an algorithm that can be found from the ITU-T recommendation I.356. Algorithms are presented in Figure 3. The algorithm on the left shows an one-point CDV which utilises only the arrival time of incoming cells. The algorithm on the right uses both the transmitting and arriving times of the cell.

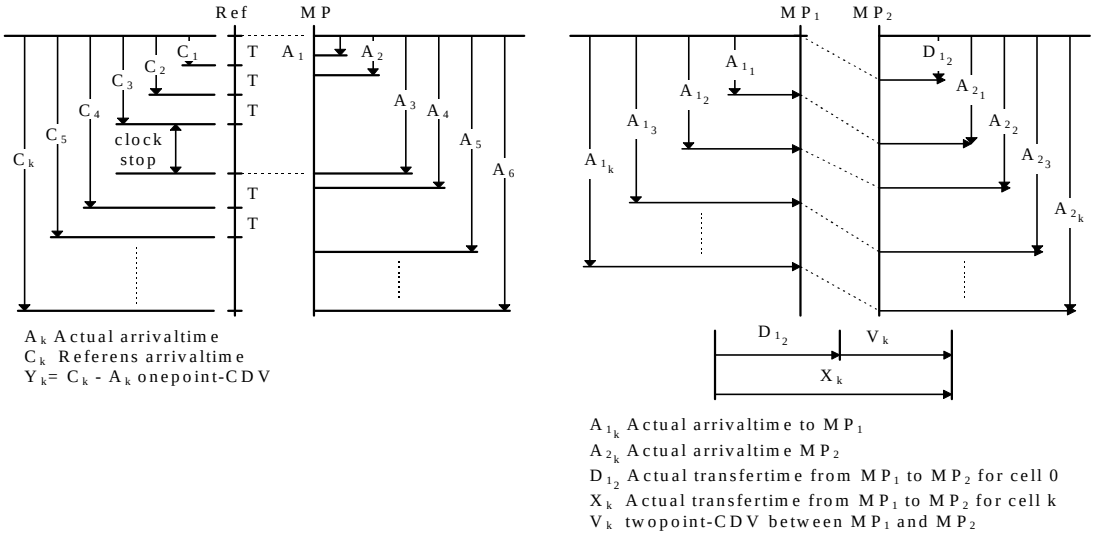


Figure 3 Evaluation of CDV from arriving cell stream [4]

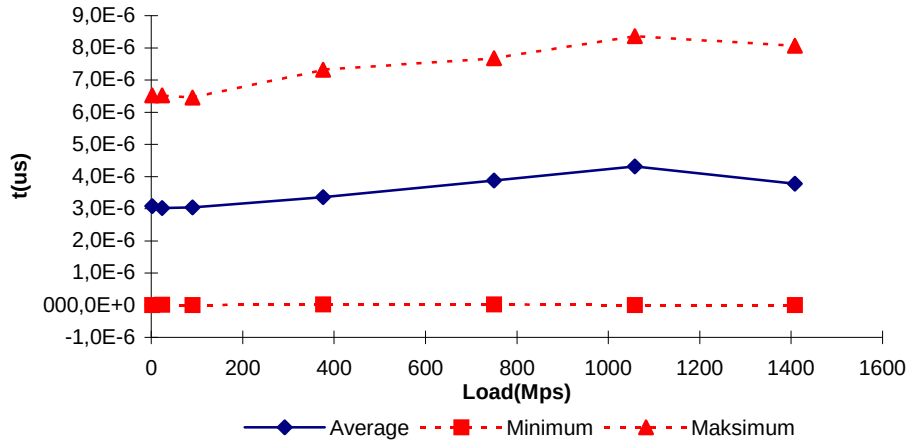


Figure 4 Switching delay variation as function of background load

3. Traffic management

3.1 Overload management

Overload situations are natural since network operations are asynchronous. In asynchronous operation cells can compete for the same time slots and therefore have to be buffered. Buffering on the other hand has to be limited, due to its cost and effect to latency - a good switch has a certain balance between latency and buffer size. If the buffer is full and there is contention switch can be seen as partly overloaded. To manage these overload situations switches have functionalities such as the Early Packet Discard Algorithm (EPDA), the Partial Packet Discard Algorithm (PPDA) and cell discarding [2, 3]

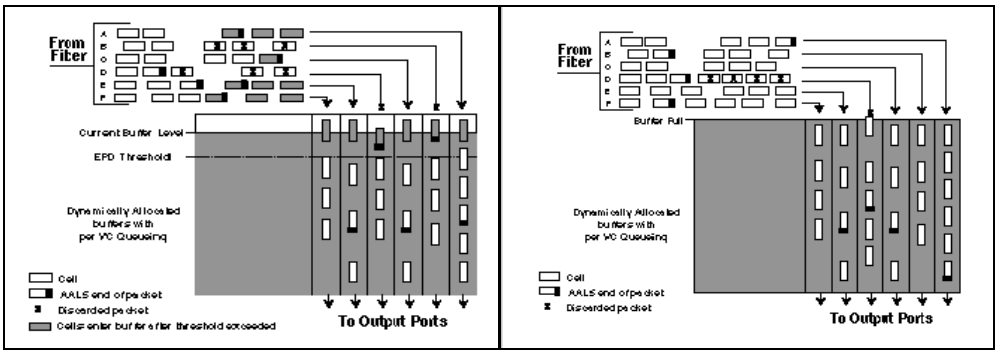


Figure 5 Working of EPD- and PPD -Algorithms [3]

These functions or procedures work under enormous stress and therefore do make mistakes. How well these work and how well they are balanced affects the whole system.

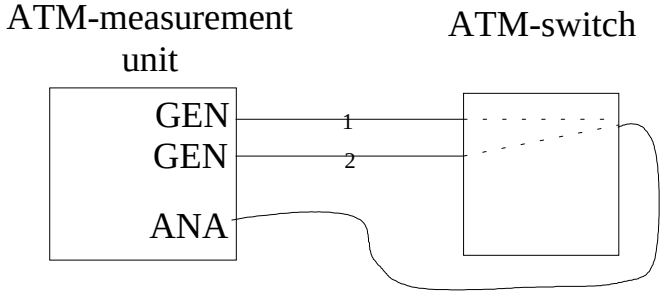


Figure 6 Connection diagram for overload measurement

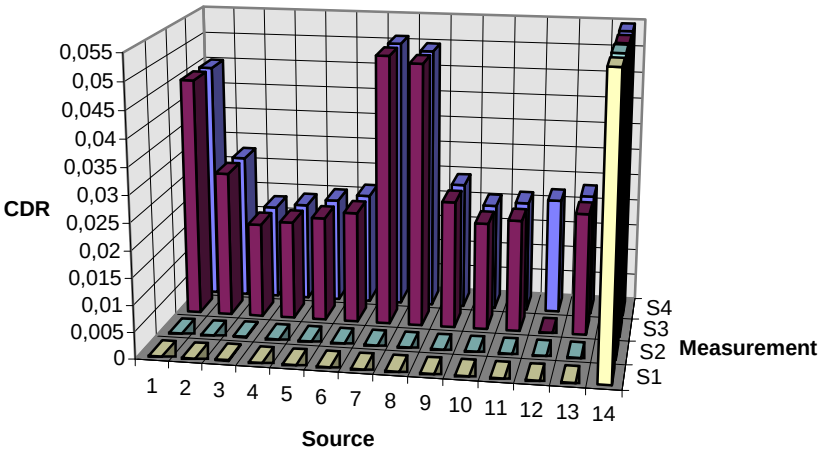


Figure 7 Cell discard ratio (CDR) for different connections under 5% overload. Connections use same sets of the traffic parameters expect connection 14 which is configured as UBR connection. Measurement series S3 and S4 are run without traffic management.

3.2 Usage Parameter Control

Usage Parameter Control (UPC) is based on the ITU-T recommendations I.356 and I.371. These recommendations present an algorithm which is used to define whether the cell is complying to the traffic contract or not. This algorithm is often called the (dual) leaky bucket algorithm [4, 5].

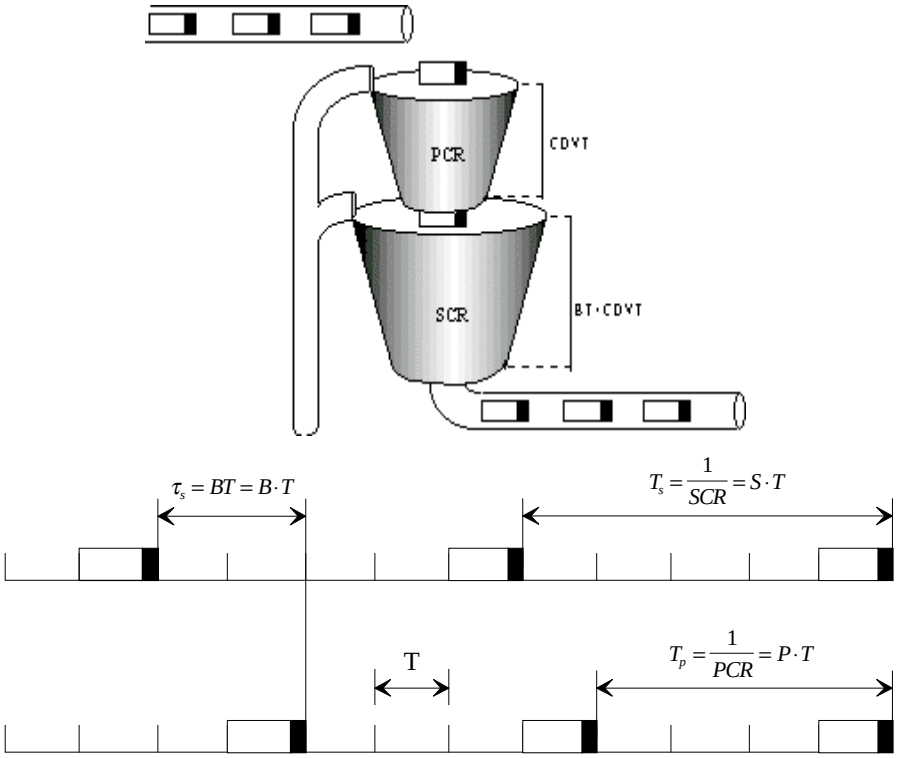


Figure 8 Dual leaky bucket construction and relation of different parameters

UPC is performed connection-per-connection so that it has great influence on the overall performance. Accuracy of the control algorithm is one of the major problems. ITU-T recommendation I.371 states that usage parameter control should be fast in response to the contract violation and it should be transparent to the connection. ATM Forum has developed a method for evaluating accuracy of the UPC. They presume that it is possible to generate strictly known traffic patterns which are then evaluated through the switch algorithm (γ_P) and the reference algorithm (γ_M). The goodness factor is then calculated as the subtraction of those two values [6]:

$$F = \gamma_M - \gamma_P \qquad (1)$$

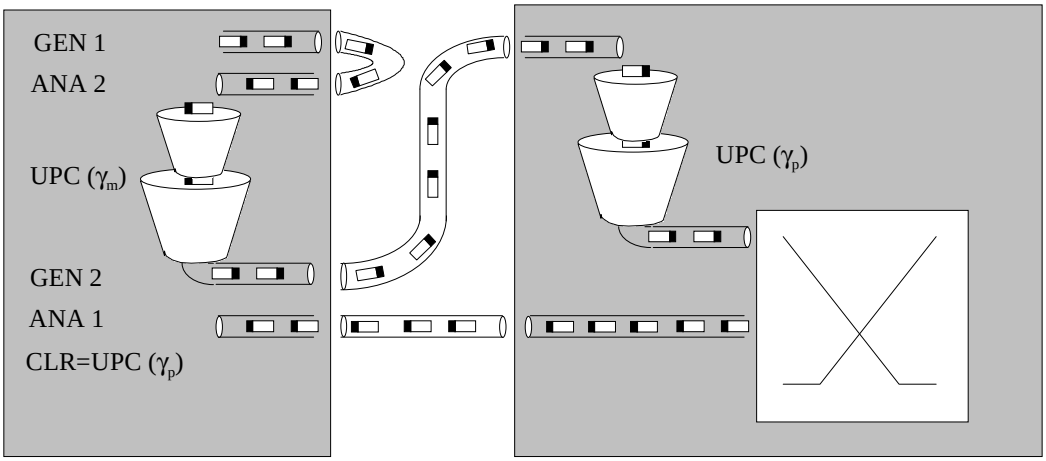


Figure 9 Usage Parameter Control connection diagram

The measurement unit ADTECH AX/4000 includes generic cell rate algorithm (GCRA) which was used in analysing the generated cell stream against the one received from the switch. The generated source pattern was an on/off source with burst size 1 (with constant bit rate) and 90…130 (with variable bit rate).

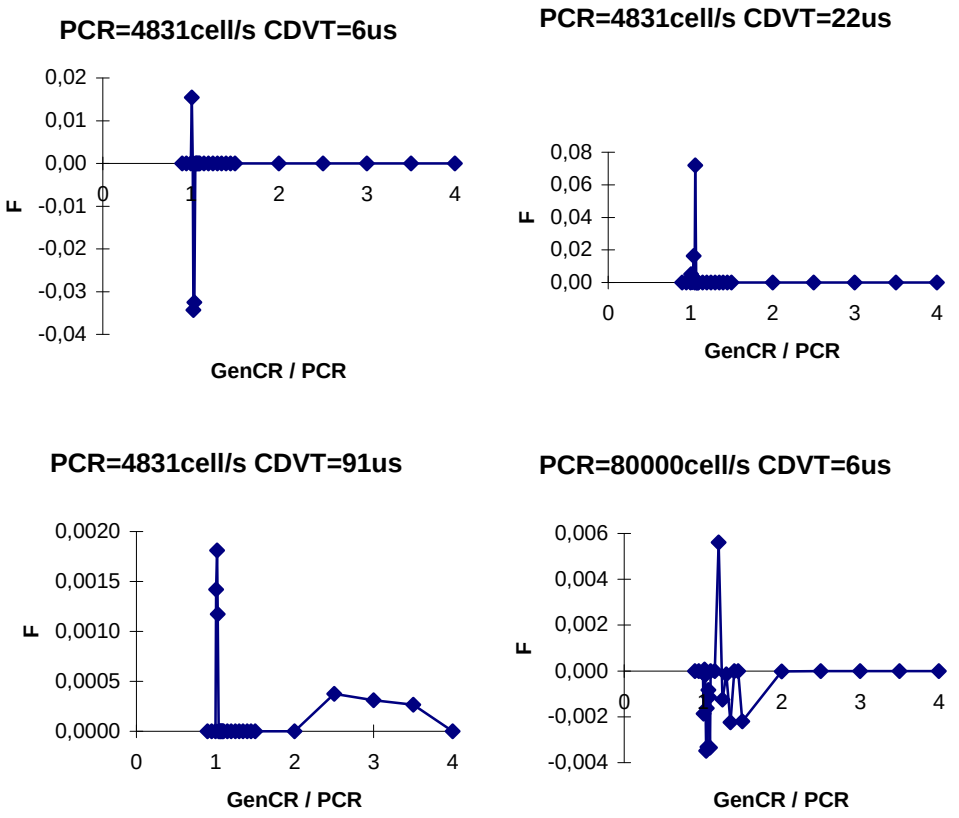


Figure 10 Goodness factor of constant bit rate policing

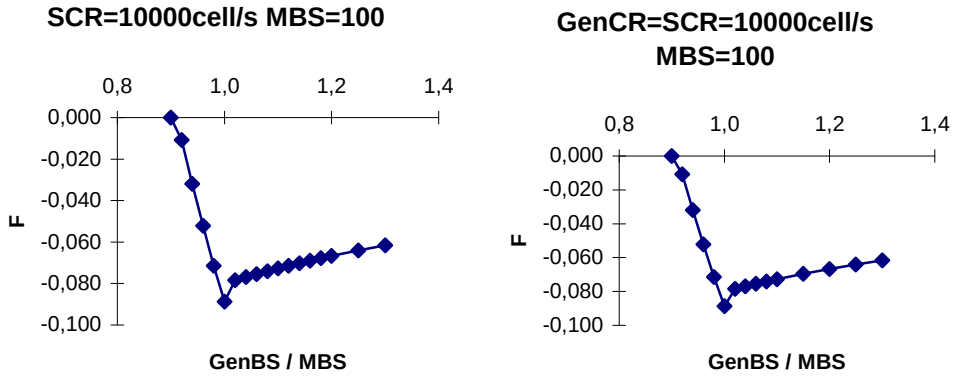


Figure 11 Goodness factor of variable bit rate policing

The most vital thing for the real world applications is the guaranteed transfer of cells. This means that the momentary fluctuations in the transmitting speed do not cause too much

policing action on the network. This is guaranteed by choosing appropriate (big enough) value for cell delay variation tolerance (CDVT). How the value should be chosen is more or less dependable of economical reasons; end devices with greater accuracy cost more than those with more fluctuation in transmitting speed. On the other hand connections with smaller CDVT on the network must have more guaranteed transmission period due to their greater vulnerability in the UPC procedure. Some guidelines can although be seen from the figures 12, 13 and [7].

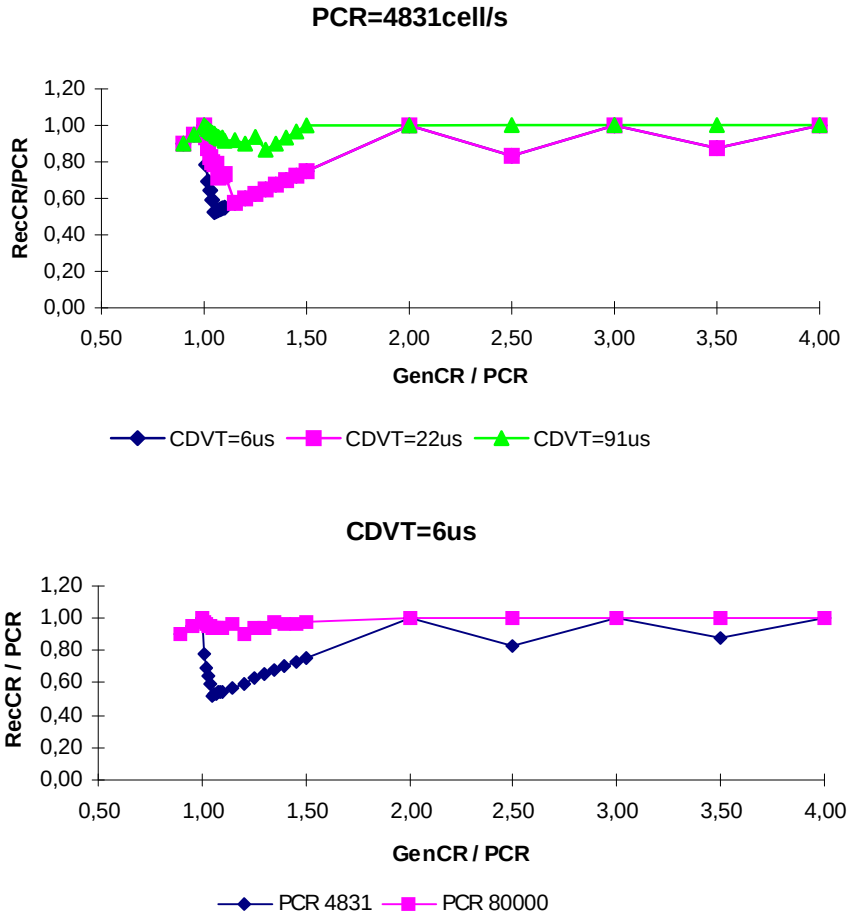
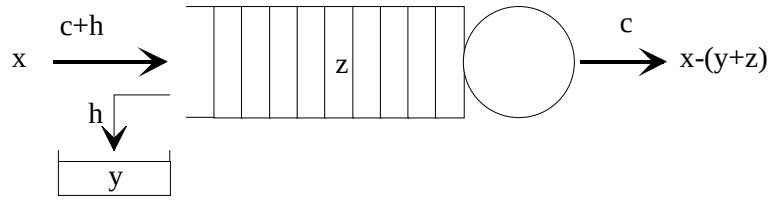


Figure 12 Received cell rate versus generated cell rate with different UPC contracts

3.3 Buffer size

The buffer size can be determined by using a predefined overload on a single link. This predefined overload will cause queue length and waiting time to grow to the maximum size of queue length - buffer size. After the maximum length is obtained the waiting time distribution will localise its maximum to that point. This can be evaluated by watching the cell transfer delay (CTD) distribution.



x.....Transmitted cells c.....Link speed

y.....Lost cells h.....Overload cells

z.....Cells on the queue

Figure 13 Buffer size measurement principle

The queue length is given by formula

$$Z = \frac{CTDmax - CTDmin}{2.8316us} \quad (2)$$

One cell transfer time 155Mbit/s SDH-link is 2,8316us.

4. Conclusions

As previous chapters showed some simple measurement techniques for performance evaluation exist. How suitable those are for real evaluation is more or less a question of what is desired. To see if the switching matrix operates correctly and efficiently, a simple transfer delay measurement gives some insight. If we like to see how traffic management operates more measurements have to be done. For the PPDA and the EPDA easy measurements can be developed. For the UPC and cell discard such measurements are presented. Results shown in this paper are actually quite ideal. FORE switch operates quite well under a heavy load and it strikes quite well in balance under overload situation. UPC procedure is implemented with an accuracy greater than expected.

For future work we intent to continue developing the measurement platform where we can run automated tests with different switches and so have more insight to what is the state of the art today. On the other hand we intent to continue some new areas which include source characterisation and developing suitable simulation models to our measurement unit.

References

/1/ ITU-T Rec. I.350 General aspects of quality of service and network performance in digital networks, including ISDNs. International Telecommunication Union. 1993. 13 s.

/2/ Holmström T. & Körner U. Two algorithms for enhancing the performance of end-to-end transport protocols on top of ATM. NTS 12, Espoo 22-24.8.1995. Espoo 1995. VTT. s. 325-338.

/3/ Fore. ForeThought Bandwidth Management. April 1995. <http://www.fore.com/html/products/whitep/FTBMWP.html>

/4/ ITU-T Rec. I.356 B-ISDN ATM layer cell transfer performance. International Telecommunication Union. 1993. 19 s.

/5/ ITU-T Rec. I.371 Traffic control and congestion control in B-ISDN. International Telecommunication Union. 1994. 32 s.

/6/ AF95-0013R10. Traffic Management Specification Version 4.0. ATM FORUM. 1995. 116 s.

/7/ Aarstad E., Kroeze J., Pettersen H. and Renger T. Experiments on Usage Parameter Control and Connection Admission Control in the Exploit Testbed. NTS 12, Espoo 22-24.8.1995. Espoo 1995. VTT. s. 155-165.