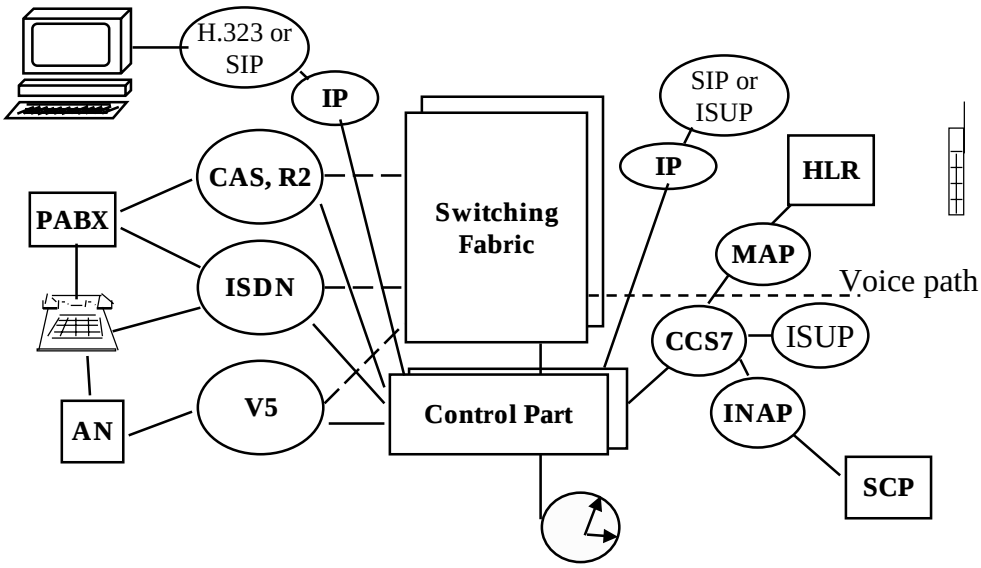
Synchronization of the Circuit switched network

ITU-T Recommendations
G.810, G.811, G.812, G.823

Summary of course scope



Timing accuracy

- ✔**UTC - Universal Time Coordinated: error is in the order of 10^{-13}**
- ✔**Error in the Primary Reference clock of the telecom network (PRC): 10^{-11}**
- ✔**Inaccuracy in frequency is classified**
  - § **Jitter (värinä): short term (> 10 Hz) changes**
  - § **Wander(vaeltelu): < 10 Hz fluctuations**
  - § **Long term frequency shift (drift or skew)**

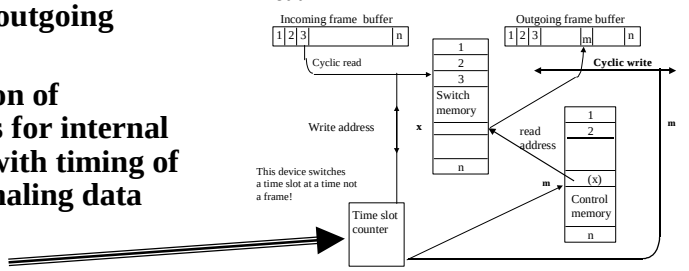
Impact of timing error

- ✔**Bit errors in regeneration**
- ✔**Quality of analogue signals deteriorates**
- ✔**Slip**
  - § **A PCM frame needs to be duplicated or is lost due to timing difference between the sender and the receiver**

Use of synchronization signals in an exchange

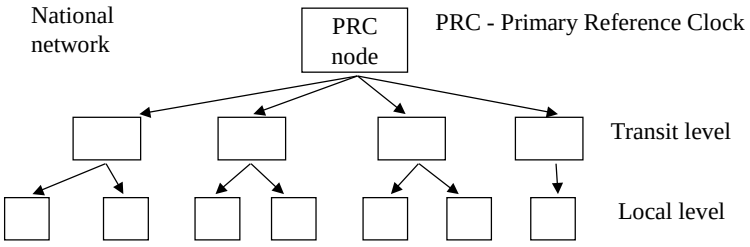
- ✔ **Synchronization of the Switch Fabric with incoming and outgoing PCM-signals.**
- ✔ **Synchronization of interface cards for internal data transfer with timing of the fabric: signaling data terminals.**

A time switch: serial write - address read



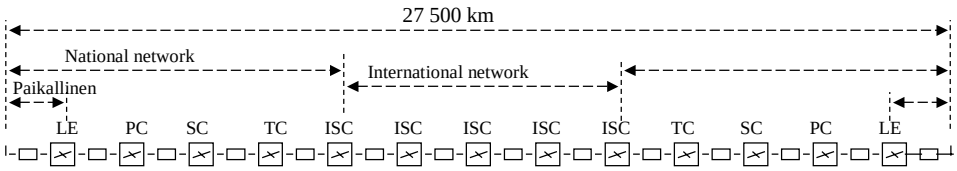
In order to reduce the timing errors and their impact on the network performance

- ✔ **Network nodes are connected to a synchronization network**
- ✔ **Slips are performed in a controlled manner**



Synchronization network is most often hierarchical. *ITU-T (G.811, G.701) also talks about mutual synchronization of clocks.*

Hypothetical reference connection



LE – Local exchange
PC – primary exchange
TC – tertiary exchange
ISC – international switching center

Digital exchange

Digital link

End to end timing requirements are set for the reference connection.
Link timing errors are additive on the end to end connection.

By synchronizing the national networks at both ends timing errors can be reduced compared to plesiochronous (based on own clocks) operation.

International connections are most times plesiochronous.

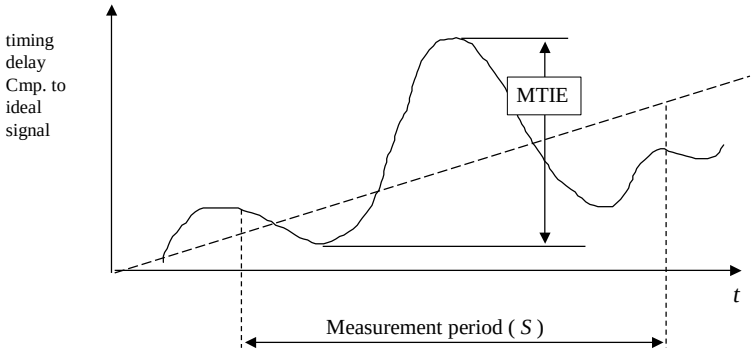
Networks can be

- ✔**Fully synchronized**
- ✔**Plesiochronous**
- ✔**Hybrids**
  - § **Are comprised of synchronized sub networks**

Plesiochronous = two connected nodes operated each based on its own clock such the they do not have a common synchronization source.

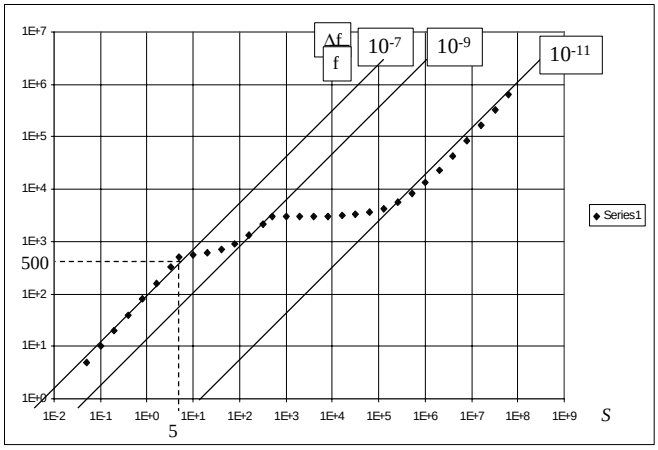
MTIE - maximum time interval error

- ✔ **the maximum of peak to peak difference in timing signal delay during a measurement period as compared to an ideal timing signal**



Maximum allowed timing error in PRC

MTIE ns



How often slips occur

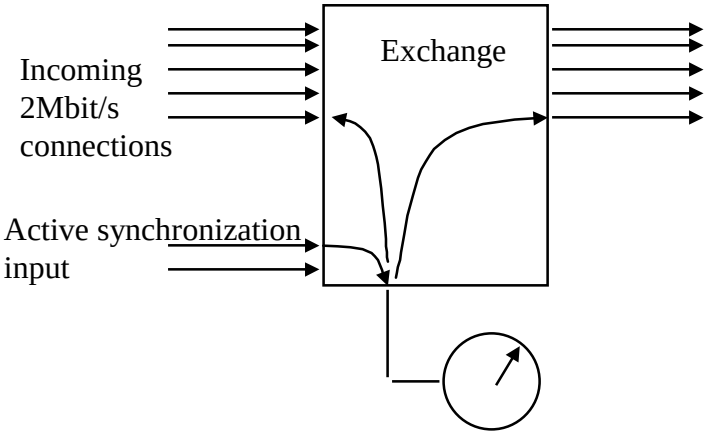
- If both ends of a connection are internally synchronized with a PRC signal theoretically slips occur not more often than once in 70 days.
- On a Reference connection a slip occurs theoretically once in 70/12 = 5.8 days or if national segments are synchronized, once in 70/4 = 17.5 days
- Slip requirement on an end to end connection is however looser:

Average frequency of slips	Share of time during 1year
less than 5/ 24h	98,90 %
5/24h . . . 30/1h	< 1%
more than 30/1h	< 0,1%

Synchronization sub-system in an exchange

- Supports both plesiochronous and slave mode operation
- Clock accuracy is chosen based on the location of the exchange in the synchronization hierarchy. Accuracy needs to go down towards the edges.
- Can synchronize itself autonomously with several PCM-signals and choose the most suitable among them (primary, secondary etc.)
- Contains a timing control algorithm (digital phase lock) that tries to eliminate
  - instantaneous timing differences caused by the transmission network (e.g. switchovers (= automatic replacement of faulty equipment by redundant))
  - jitter
  - and follow smoothly the incoming synchronization signal

Slips occur on connections whose timing differs from the timing signal used by the exchange

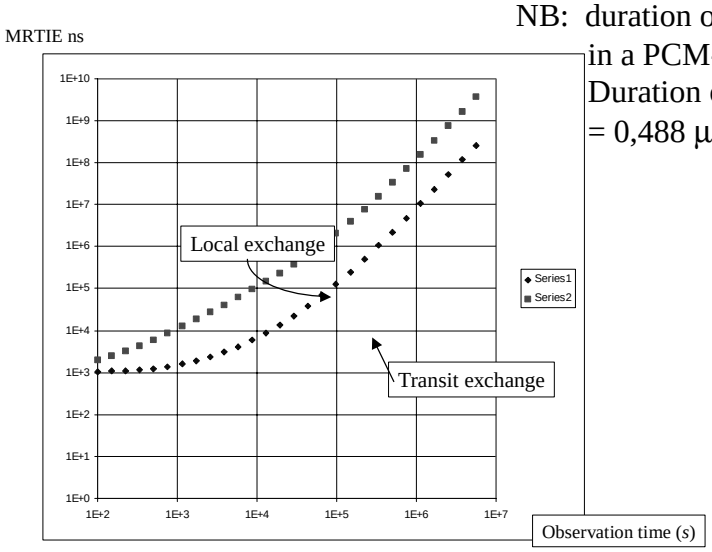


Exchange clock follows the synchronization signal

- Relative error is used to set requirements: MRTIE - maximum relative time interval error : MRTIE ≤ 1000 ns ($S \geq 100$s).
- Requirement says how well the exchange must follow the synchronization signal when the input is practically error free.
- When none of the synchronization inputs is good enough, the exchange clock automatically switches over to plesiochronous operation
- In plesiochronous mode the relative error in the exchange MRTIE ≤ (a S + 1/2 b S^2 + c) ns (see following slide).
- System monitors all inputs continuously and when a quality signal is detected, either automatically or by an operator command the system switches back to slave mode.

MRTIE in an exchange in the plesiochronous mode

NB: duration of a time slot in a PCM-signal is 3.9 μs. Duration of a bit = 0,488 μs = 488 ns.



Stability of the exchange clock

Stability is measured by ageing (=*b*) – for a temperature stabilized crystal ageing is in the order of $n \times$ 10exp-10/day.

MRTIE ≤ (a S + 1/2 b S^2 + c) ns, S = measurement period, and
a = accuracy of intial setting of the clock.

	Transit node clock	Local node clock
a	0.5 corresponds to an initial frequency shift of 5×10^{-10}	10.0 1×10^{-8}
b	1.16×10^{-5} corresponds to ageing 10^{-9} /day	2.3×10^{-4} corresponds to ageing 2×10^{-8} /day
c	1000	1000